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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/921,022 | 08/02/2001 | Guy Harlan Humphrey | 10010504-1 | 7798 |

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AGILENT TECHNOLOGIES, INC.
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| EXAMINER |
|---|
| NGUYEN, MINH T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 06/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/921,022 | HUMPHREY, GUY HARLAN | |
| | Examiner | Art Unit | |
| | Minh Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment filed on 4/22/02 has been received and entered in the case. The amendment presented therein overcomes the informality objections, and therefore, are withdrawn. The prior art rejections are maintained and repeated for the reasons set forth below. This action is FINAL.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,568,062 to Kaplinsky.

As per claim 3, Kaplinsky discloses an apparatus (Fig. 1) for reducing the slew rate of transition edges of a digital signal (the signal OUTPUT at the node terminal 20) on a node 20 of an integrated circuit, comprising:

a first switchably conductive device 17 characterized by a first threshold voltage (the threshold voltage of transistor 17) wherein the first switchably conductive device 17 connected between the node 20 and a voltage source VSS and responsive to a driving signal INPUT, the

functional recitation on lines 5-10 is met because the first switchably conductive device 17 is an NMOS transistor; and

a second switchably conductive device 15 characterized by a second threshold voltage (the threshold voltage of transistor 15) which is greater than the first threshold voltage (the width of transistor 15 is 120 and transistor 17 is 680 and the lengths are the same, column 5, lines 5-6), wherein the second switchably conductive device 15 connected between the node 20 and the voltage source VSS and responsive to the driving signal INPUT; the functional recitation on lines 5-10 is met because the second switchably conductive device 15 is an NMOS transistor.

As per claim 4, the recited limitation is met because transistors 15 and 17 are FETs.

As per claim 1, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Kaplinsky teaches the circuit, he inherently teaches the method. Note that in the recited first and second input signals are the digital signal as discussed in claim 3. The recited first and second input signals can also interpreted as the signals to the gates of transistors 17 and 15, respectively, as shown in Fig. 1; and the step recited on the last three lines is met because the drains of transistors 15 and 17 are connected together.

As per claim 7, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Kaplinsky teaches the circuit, he inherently teaches the method.

As per claim 8, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Kaplinsky teaches the circuit, he inherently teaches the method wherein the monitoring a level step is performed by transistors 15 and 17, i.e., using the first and second threshold voltages characteristics, when the level of the driving voltage is lower than the

monitor level threshold voltage, do not conduct, when the level of the driving voltage is equal or higher, perform the conducting function; the stepping up conduction of current to the node step when the level reaches a first threshold voltage is performed by transistor 17, and the stepping up conduction of current to the node step when the level reaches a next threshold voltage is performed by transistor 15.

3. Claims 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,877,647 to Vajapey et al.

As per claim 10, Vajapey discloses a method for controlling the slew rate of transition edges of a digital signal on a node 160 of an integrated circuit (Fig. 6), the method comprising the steps of:

monitoring a level of a driving voltage (use the threshold voltages of transistors P1 and P2 as first and second threshold levels);

when the level reaches a first threshold voltage, stepping down conduction of current to said node (gradually turn off the conduction of transistor P1);

when the level reaches a next predefined threshold voltage (the second threshold level), stepping down conduction of current of said node (gradually turn off the conduction of transistor P2).

As per claim 11, Vajapey further teaches that by adding more PMOS transistors to the circuit of Fig. 6, the slew rate of the digital signal can be more controlled (column 7, lines 1-5), i.e., repeating the second stepping down step for the additional next predefined threshold voltages.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,568,062 to Kaplinsky in view of US Patent No. 5,877,647 to Vajapey et al.

As per claim 5, Kaplinsky teaches an apparatus (Fig. 1) for reducing the slew rate of a digital signal which comprises first and second switchably conductive devices having first and second threshold voltages as discussed in claim 3 above but he does not explicitly teach an apparatus which comprises one or more additional switchably conductive devices wherein each has different threshold voltage as called for in the claim.

Vajapey discloses an apparatus (Fig. 6) for controlling the slew rate of an output signal wherein the switchably conductive devices P1 and P2 have different threshold voltages, and in column 7, lines 1-5, he explicitly suggests to implement another embodiment which has one or more additional switchably conductive devices to further control the slew rate of the digital signal at the node.

It would have been obvious to one skilled in the art at the time of the invention was made to add one or more switchably conductive devices to the Kaplinsky's circuit wherein each has different threshold voltage.

The motivation/suggestion for doing so would have been obvious for the reason discussed herein above, i.e., more control of the slew rate of the digital signal at the node 20 of the Kaplinsky's circuit.

Therefore, it would have been obvious to add one or more additional switchably conductive devices wherein each has different threshold voltage to the Kaplinsky's circuit shown in Fig. 1 to obtain the invention specified in the claim.

As to the functional limitation recited on lines 7-12 of the claim, the recitation is merely the operation of a typical NMOS transistor, and therefore, it is met when one or more additional NMOS transistors are added to the circuit.

As per claim 6, the recited limitation is met because the first, second and one or more additional switchably conductive devices are NMOS transistors.

As per claim 2, this claim is rejected for the same reasons noted in claim 5.

As per claim 9, this claim is rejected for the same reason noted in claim 5 wherein the recited stepping up step for one or more additional next predefined threshold voltages are performed by the one or more additional transistors as discussed in claim 5.

### *Response to Arguments*

5. Applicant's arguments filed on 4/22/02 have been fully considered but they are not persuasive.

Regarding the argument that Kaplinsky does not teach or suggest that the threshold voltages of the two transistors 15 and 17 are actually different from one another. The examiner notes that as discussed in the preceding rejections, this limitation is met since the size of

transistor 15 is different from the size of transistor 17. The Applicant is further referred to MPEP 2112.01 which states that when the structure recited in the claim is substantial identical to that of the reference, claimed properties and functions are presumed to be inherent and the Applicant has the burden of showing that the reference circuit does not process the properties/functions which recite in the claim. In this case, in order for the argument to be persuasive, the Applicant needs to show that, in all cases, the claimed circuit is not anticipated by the Kaplinsky circuit when transistors 15 and 17 having different sizes are used, i.e., in all cases, picking two transistors 15 and 17 having different sizes to implement the Kaplinsky circuit, these transistors must not process the properties, which have different threshold voltages, recited in the claim.

Regarding the argument that Robert Pierret, a well-respected authority in the area of semiconductor devices, does not mention anything about varying the size of a transistor for changing the threshold voltage of the transistor in his book regarding "threshold considerations", therefore, varying the size of a transistor does not change the threshold voltage of the transistor. This argument is not found persuasive because there are no guarantee that the author covered all the possibilities about this topic in his book.

Regarding the argument that Vajapey merely teaches that the trigger point for turning on P1 and P2 in succession is a delay time, and nowhere in the Vajapey reference mentions that the threshold voltages of transistors P1 and P2 are actually different. The examiner notes that since P1 and P2 have different sizes, they have different threshold voltages (as discussed herein above), and since the gates of these transistors are both received the same input signal, the transistor which has a lower threshold voltage will be ON first, and after a delay time, i.e., the

time for the input signal to raise from the first threshold voltage to the second threshold voltage, the other transistor will be ON next, and the recited limitation is met.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MN
June 7, 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800